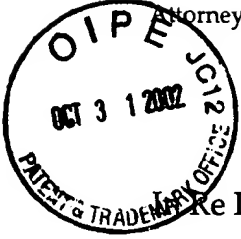


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Attorney's Docket No. 004120.P005

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Patent Application of:

Jengsheng Jason Cong et al.

Examiner: Unknown

Application No.: 09/823,085

Art Unit: 2123

Filed: March 29, 2001

For: Method and Apparatus for
Calculation of Crosstalk Noise in
Integrated Circuits

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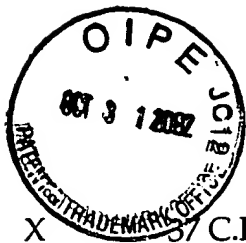
INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):



X 37 C.F.R. §1.97(b); OR

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If there are any additional charges, please charge Deposit Account No. 02-2666.
Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/20/02


Michael J. Mallie, Reg. No. 36,591

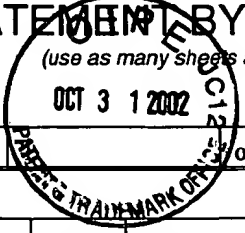
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	A	KAWAGUCHI, H. et al.: "Delay and Noise Formulas for Capacitively Coupled Distributed RC lines", in Proc. Asia and South Pacific Design Automation Conf., pp. 35-43, 1998.													
	B	NAKAGAWA, S. et al.: "On-chip Cross Talk Noise Model for Deep-Submicrometer ULSI Interconnect", Hewlett-Packard Journal, vol. 49, pp. 39-45, Aug. 1998.													
	C	STÖHR, T. et al.: "Analysis, Reduction and Avoidance of Crosstalk on VLSI Chips", in Proc. Int. Symp. On Physical Design, pp. 211-218, April 1998.													
	D	VITTAL, A. et al.: "Crosstalk Reduction for VLSI", IEEE Trans. On Computer-aided Design of Integrated Circuits and Systems", vol. 16, pp. 290-98, 1997.													
	E	DEVGAN, A. : "Efficient Coupled Noise Estimation for On-chip Interconnects", in Proc. IEEE/ACM Int. Conf. On Computer Aided Design, pp. 147-153, 1997.													
	F	SEMICONDUCTOR INDUSTRY ASSOCIATION, "The National Technology Roadmap for Semiconductors", 1997 edition.													
	G	SHEPARD, K.L., et al.: "Noise in Deep Submicron Digital Design", in Proc. IEEE/ACM Int. Conf. On Computer Aided Design, pp. 524-531, 1996.													
	H	SAKURAI, T.: "Closed-form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSIs", IEEE Trans. On Electron Devices, vol. 40, pp. 118-124, 1993.													

Examiner Signature	Date Considered	
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